WHAT IS CLAIMED IS:

1. A control circuit for testing a memory control module, said memory control module comprising first and second memory blocks, said control circuit comprising:

a processing unit executing a memory testing program specific to said first memory block, and asserting data read/write commands; and

a control chip in communication with said processing unit and said memory control module, accessing to said second memory block of said memory control module for test in response to said data read/write commands in a first state.

2. The control circuit according to claim 1 wherein said control chip accesses to said first memory block of said memory control module for test in response to said data read/write commands in a second state.

3. The control circuit according to claim 2 further comprising a mapping circuit for switching said data read/write commands between said first and second states and mapping said data read/write commands in said first state onto said second memory block of said memory control module.

4. The control circuit according to claim 3 wherein said processing unit and said control chip are a central processing unit and a north bridge chip of a computer system, respectively, said mapping circuit is included in said north bridge chip, and said first and second states are different logic states.

5. The control circuit according to claim 2 wherein said control chip changes the level of a specific address line between said control chip and said memory control module to different values so as to switch said read/write commands between said first and second states.

6. The control circuit according to claim 2 wherein said first memory block includes 2^n addresses, said control circuit comprises n counts of address lines

corresponding to said read/write commands and at least one specific address line between said control chip and said memory control module for indicating states of said read/write commands.

7. The control circuit according to claim 6 comprising one said specific address line to indicate high-level and low-level states of said read/write commands as said first and second states.

8. The control circuit according to claim 7 wherein said second memory block has the same address space as said first memory block and designated with higher addresses than said first memory block.

9. The control circuit according to claim 8 wherein the value n is equal to 32, and each of said first memory block and said second memory block has a 4-GB address space.

10. The control circuit according to claim 6 comprising m counts of specific address lines, where m is greater than one, to indicate 2^m counts of states of said read/write commands for testing third memory blocks of said memory control module in addition to said first and second memory blocks.

11. The control circuit according to claim 10 wherein the value n is equal to 32, and each of said first, second and third memory blocks has a 4-GB address space.

12. The control circuit according to claim 2 further comprising switch-setting means for determining when said first and second states are entered, respectively.

13. The control circuit according to claim 12 wherein said switch-setting means is the BIOS of a computer system or a timer.

14. A control circuit for testing a memory control module of a computer system, said memory control module comprising at least first and second memory blocks, said control circuit comprising:

a central processing unit asserting data read/write commands for testing said

first memory block of said memory control module;

a north bridge chip in communication with said central processing unit and said memory control module, having said first memory block of said memory control module respond to said data read/write commands to be tested at a first time point; and

a mapping circuit in communication with said memory control module, mapping said data read/write commands onto said second memory block of said memory control module to have said second memory block respond to said data read/write commands to be tested at a second time point.

15. The control circuit according to claim 14 wherein said mapping circuit is incorporated into said north bridge chip.

16. The control circuit according to claim 15 further comprising at least one specific address line between said mapping circuit and said memory control module, which have different logic states at said first and second time points.

17. A control method for testing a memory control module, said memory control module having an address space greater than the testing limit of a memory testing tool, said control method comprising steps of:

dividing said memory control module into at least a first memory block and a second memory block, each of said memory blocks having an address space within the testing limit of said memory testing tool;

having said first memory block respond to data read/write commands asserted in response to said memory testing tool in a first situation; and

having said second memory block respond to said data read/write commands in a second situation.

18. The control method according to claim 17 wherein said first and second memory blocks are identical in address space and said second memory block is

designed with higher addresses than said first memory block.

19. The control method according to claim 18 wherein said memory testing tool is specific to the test of said first memory block.

20. The control method according to claim 19 further comprising a step of mapping said data read/write commands onto said second memory block in said second situation.

21. The control method according to claim 20 wherein the testing limit of said memory testing tool is 4 GB, and said memory control module is divided into a plurality of memory blocks, each having a 4-GB address space.

22. The control method according to claim 19 wherein said first situation indicates a first logic state of said read/write commands, and said second situation indicates a second logic state of said read/write commands different from said first logic state.

23. The control method according to claim 22 wherein said first and second situations are switched in response to a timing result.

24. The control method according to claim 22 wherein said first and second situations are switched according to the settings in the BIOS.

25. The control method according to claim 22 wherein said memory control module is divided into more than two memory blocks, and more than two different logic states are sequentially imparted to said read/write commands to have said memory blocks respond to said read/write commands in turn.

26. The control method according to claim 22 wherein said first and second logic states of said read/write commands are determined by a mapping circuit incorporated in a north bridge chip and coupled to said memory control module.

27. The control method according to claim 26 wherein said memory testing tool is executed and said read/write commands are asserted by a central

processing unit in a big real mode.